DESIGN, CHARATERIZATION, COMPARISON OF ULTRA LOW POWER HIGH SPEED CMOS INVERTER AT 90NM/65NM/45NM/32NM/22NM/16NM

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Abstract

Numerous efforts have been made to minimize power dissipation and to balance the tradeoff between power, area, and delay at 90nm/65nm. Paper presents a bit forward in this direction and tries to concentrate on power as well as on performance. In the present work simulation of CMOS inverters below threshold at **16nm /22nm /32nm / 45nm / 65nm / 90nm** using TANNER tool is done and tries to optimize delay and noise along with power. Also the device size calculated in each case and for achieving ultra Low power, voltage scaling and operation in threshold are utilized. STACK is also reviewed and can be used where delay and area not matters. Further optimization of the results is done by employing DTMOS. This work tries to maintain delay in limits with continuous scaling down the technology files and the supply voltage.

Keywords: Sub threshold operation, CMOS inverter, Ultra Low power, DTMOS, 16nm technology.

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1 INTRODUCTION

Today's everyone needs devices which have longer battery life, consumes less power, and have high speed and that too in small dimensions. Thus Power, Area, Delay are the three important parameters of today's VLSI design. Unfortunately, if one tries to optimize a parameter then cost paid would be in terms of degradation of other parameters. As for example if one's tend to decrease the power by decreasing the supply voltage or by operating a transistor in sub-threshold region, this results in increase in delay. Thus a proper design requires a balanced tradeoff between power, area, and delay. This paper focuses on design techniques for low power and high speed operation depending on required application for CMOS inverter as it is the most basic part of all design. Once its operation and properties are clearly understood designing more complex structures are relatively easy. In the present work tanner tool is used for our results at 90nm, 65nm, 45nm, 32nm, 22nm, 16nm technology files.

Next thing which is the major requirement for the circuit design is low power Consumption. There are two components that establish the amount of power dissipated in a CMOS Circuit. These are static dissipation – due to leakage current and dynamic dissipation – due to short circuit current and due to charging and discharging of load capacitances (transient component) [2]. Static power dissipation is mainly due to reverse bias drain-substrate (-well) pn junction leakage current from transistors in the off state. The deep –submicron off state current is sub threshold leakage and it dominates with technology scaling [3]. These components can be expressed mathematically as below:

$$P_{total} = P_{dynamic} + P_{static} \quad \ldots\ldots\ldots\ldots\ldots\ldots(1)$$

$$P_{dynamic} = C_l V_{dd}^2 f \quad \ldots\ldots\ldots\ldots\ldots\ldots(2)$$

$$P_{static} = \sum_{i=0}^{n} \text{leakagecurrent} \times \text{supply voltage}$$

$$\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

Where, n= number of devices.

C_l= load capacitance

f = switching frequency

V_{dd}= supply voltage

The important factor that can be seen from above that power dissipation is proportional to switching frequency and independent of device parameters. Thus depending on above equations,

main solution to decrease the power consumption is to decrease the supply voltage and also reduce the switching frequency and leakage current (that flows in off state of MOS device). Till now various techniques had been employed to decrease the power dissipation such as simply scaling down voltage supply, VTCMOS, MTCMOS, STACKING scheme. This Paper entirely concentrates on operating in sub threshold and DTMOS technique for ultra low power results and STACK scheme is ignored here because of extra delay and area factors. This paper is organized as follows. Section 1 already gives a general introduction about power dissipation and its sources and the work already done. Section 2 focuses on various design techniques that exist and can be used to optimized results such as noise margin, propagation delay, Power dissipation. Section 3 presents simulation results. In Section 4 paper is concluded and Section 5 is of references made to write this paper.

2 DESIGN TECHNIQUES

2.1 Maximizing Noise Margin

The noise margin of a digital gate or circuit indicates how well the gate or circuits will perform under noisy conditions[8]. Two noise margins are defined; one corresponding to logic high (NM_H) and other corresponding to logic low (NM_L).These are defined mathematically as (and are shown in fiure 1)

$NM_H = V_{IH} - V_{OH}$ …….(4)

$NM_L = V_{IL} - V_{OL}$ …….(5)

Where, V_{IH} = Minimum input voltage which can be interpreted as logic "1"

V_{OH} = Maximum output voltage when the output level is logic "1"

V_{IL} = Maximum input voltage which can be interpreted as logic logic"0"

V_{OL} = Minimum output voltage when the output level is logic "0"

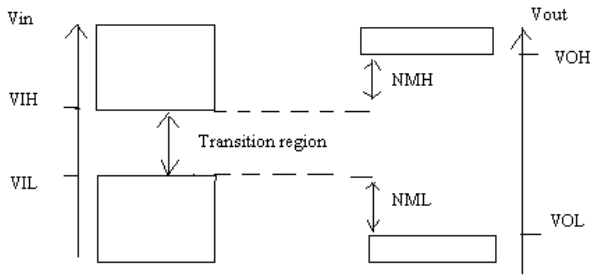

Figure 1 Definition of Noise margins

For maximizing the noise margin and to obtain symmetrical DC characteristics it is preferable to make driving strengths of both PMOS & NMOS equal. This can be done by making PMOS device wider than NMOS device. This places the switching threshold of Inverter at $V_{dd}/2$.Switching Threshold of inverter is a point where $V_{in} = V_{out}$.. Switching threshold can be varied by varying the W_p/W_n ratio. Changing this ratio shifts the transient region of VTC and this may be useful is some applications where there is much input noise and by increasing the ratio we can make output independent of input noise. For the most cases and for simulation results in this paper, the low and high noise margins are maximized and are set equal.

2.2 Minimizing Propagation Delay

Propagation delay is the delay after which change in input is presented to output. It can be calculated as

$$\tau = (\tau phl + \tau plh)/2 \quad \text{.....(6)}$$

Where τphl is the time delay between the V(50%)-transition of the rising input voltage and the V(50%)-transition of the falling output voltage. Similarly τplh is the time delay between the V (50%)-transition of the falling input voltage and the V(50%)-transition of the rising output voltage[4]. Above mentioned technique of widening PMOS to obtained symmetrical characteristics aimed at equating the high to low and low to high propagation delay. But this not yields the minimum propagation delay. If noise margin is not of utmost importance then propagation delay can be minimized by reducing the width of PMOS device [1]. This is so because when PMOS width is scaled up besides improving low to high propagation delay it degrades the high to low propagation delay because of a larger parasitic component.

2.3 Minimizing Power

2.3.1 Voltage Scaling

A simpler way to decrease the power dissipation is to decrease the supply voltage as mentioned in equation 1 and 2 above which shows that average power dissipation is proportional to the square of power supply voltage. Neglecting second order effects such as sub threshold conduction, it can be seen that the CMOS inverter will continue to operate correctly with a supply voltage which is as low as the following limit value

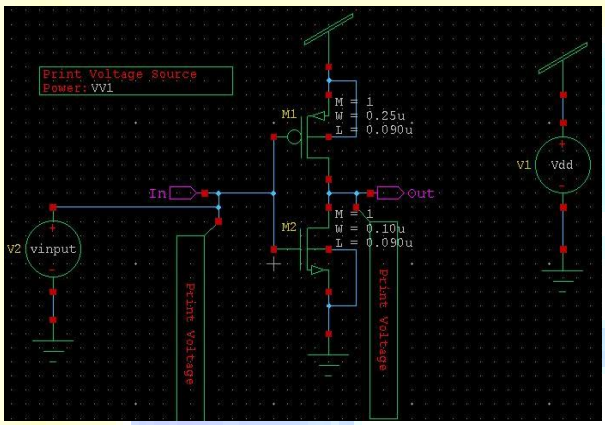

Figure 2 conventional inverter

$$V_{dd}^{min} = V_{tn} + |V_{tp}| \quad \ldots\ldots\ldots\ldots\ldots\ldots(7)$$

Although this technique reduces the dynamic power dissipation, the unavoidable design tradeoff is the increase of delay. Figure 1 shows the conventional inverter and in figure 2 simulation waveforms are shown. It can be seen that with decreasing voltage power is reduced with not much effect on DC characteristics of Inverter.

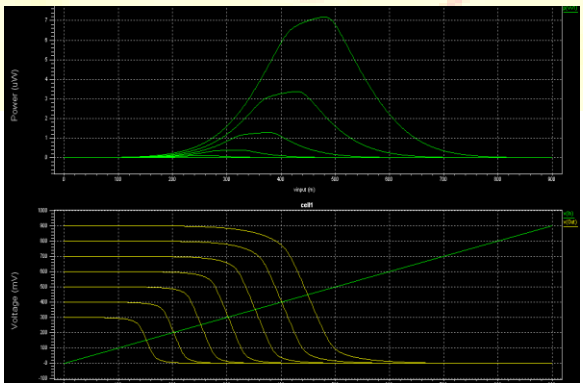

Figure 3 DC Characteristics and average power dissipation at different supply voltages

2.3.2 Sub-threshold Operation

Sub threshold region of operation for an MOS Transistor occurs when the gate to source voltage of a transistor is biased under the threshold voltage. The reason of operating the circuit in sub threshold mode is to able to exploit the sub threshold leakage current as the operating drive current.This current is high enough to switch the gate between low and high levels and provide sufficient gain to produce acceptable VTC's [1].Very low value of switching currents causes a very slow operation but this might be acceptable for some applications and simulation results shows saving in power outweighs the increase in delay.

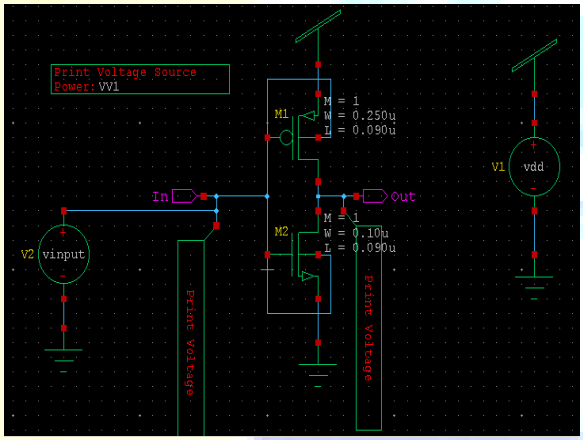

Figure 4 Inverter with substrate terminal connected to gate terminal.

For sub threshold operation V_{dd}^{min} must be 2 to 4 times of kT/q(=25mv at room temperature). Therefore we observe a major deterioration below 100mv. Thus above boundary condition suggests that only possible way to opearate circuits below 100mv is to cool the circuit or reduce the ambient temperature. Figure 3 shows the inverter circuit for subthreshold operation where body effect is intentionally included to minimize leakage power.

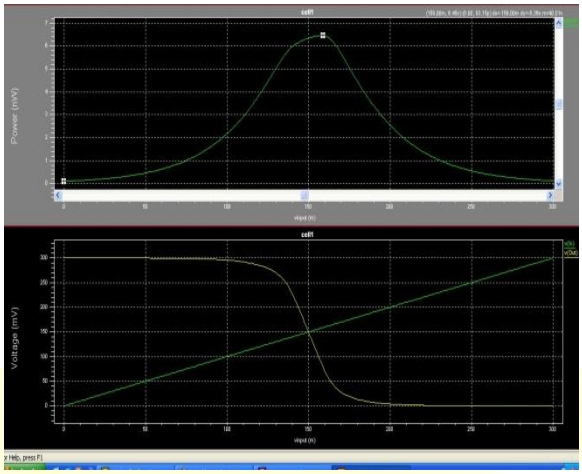

Figure 5 DC characteristics & average Power Dissipation(at 65nm)

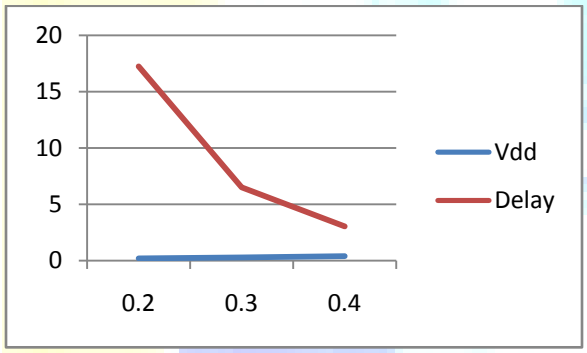

Figure 6 Delays vs. V_{dd} (at 22nm)

2.3.3 DTMOS

In this technique gate terminal and substrate terminal of the MOS devices are shorted to include body effect as a advantage. This technique minimizes the leakage power dissipation. When inverter receives logic 1 as input the PMOS device is off and PMOS gate and substrate terminal are connected to logic 1 which causes the shift in threshold voltage of PMOS thereby decreasing the leakage current and leakage power dissipation. Similarly when inverter receives a logic 0 input then NMOS device is off and gate and substrate terminal of NMOS are shorted which causes a increase in threshold voltage of NMOS thereby decreasing leakage current and leakage power dissipation. In this paper all the above techniques are utilized simultaneously to arrive at ultra low power, optimized noise margin, optimized delay solution. This technique can't be used

for $V_{dd\ greater}$ than 0.5-0.7 V because doing so would make the body to source junction forward biased and the device would no longer behaved as MOS device.

2.3.4 STACK APPROACH

In this approach of reducing power dissipation, a transistor is broken down into two half size transistors. When these two half transistors are in off condition together, induced reverse bias between these two transistors results in sub threshold leakage current reduction and hence reduction in power dissipation[7]. Figure 7 shows the structure of STACK approach and Figure 8 shows the DC results obtained with this approach for a technology file of 45nm. It was observed that a good power reduction is obtained by this approach but at the cost of induced delay and area. As it can be seen that power dissipation at 0.4V for 45nm bulk technology files is just 6.94nw as compared to 23.31nw (as shown in table 1) without stack approach. Thus this technique could be used only where delay and area not matter and power is the main concern.

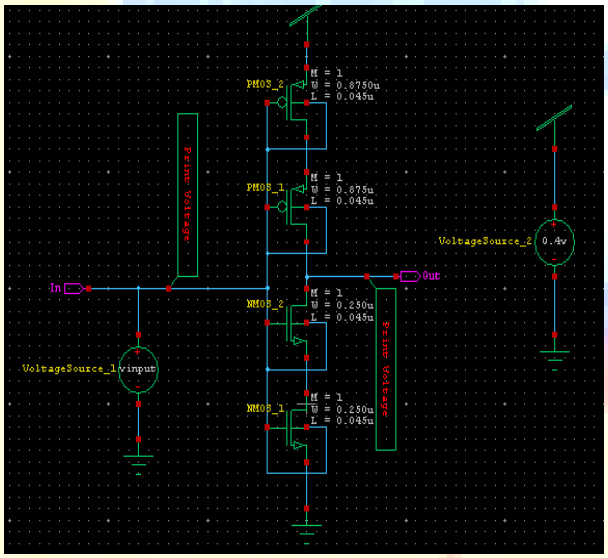

Figure 7 STACK approach

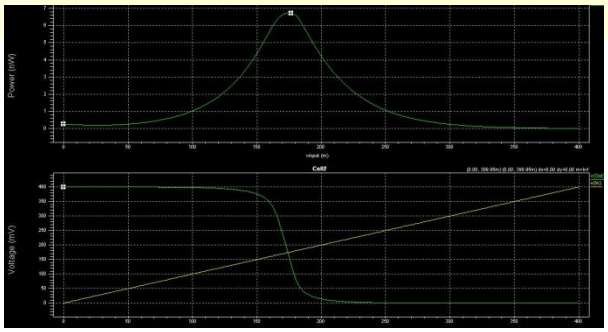

Figure 8 DC characteristics & average Power Dissipation (at 45nm) for STACK approach.

3 SIMULATION RESULTS

Tanner Tool has been used for calculating Power, Delay and plotting DC and Transient Characteristics of Inverter at 16nm, 22nm, 32nm, 45nm, 65nm, 90nm. Below are the waveforms for 16nm and other results are tabulated in Table 1.

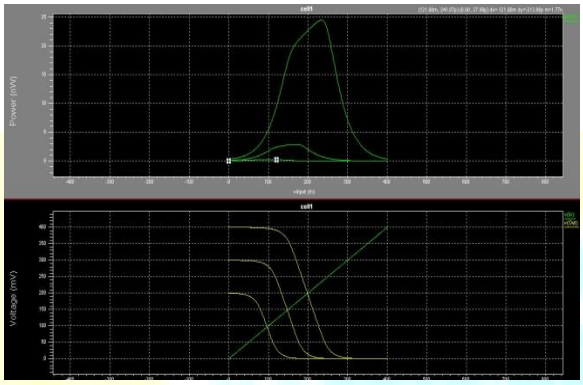

Figure 9 DC characteristics & average Power Dissipation (at 16 nm)

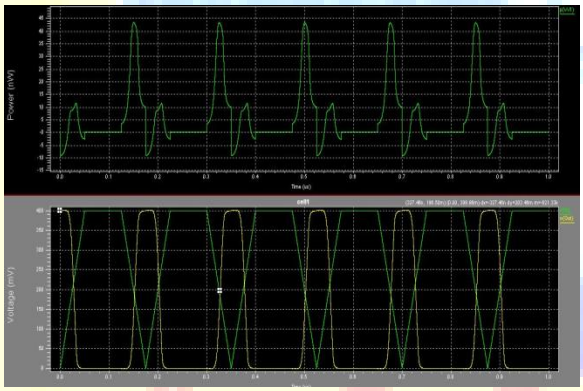

Figure 10 Transient characteristics & Power Dissipation at 0.4V (at 16 nm)

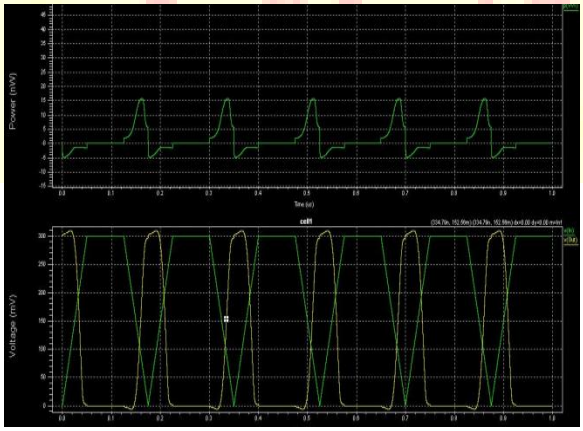

Figure 11 Transient characteristics & Power Dissipation at 0.3V (at 16 nm)

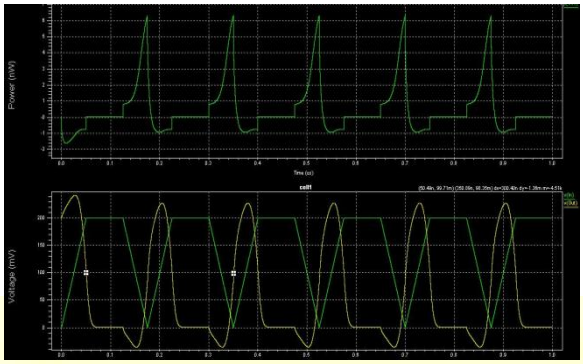

Figure 12 Transient characteristics & Power Dissipation at 0.3V (at 16 nm)

It can be seen from above results that the characteristics are good enough for circuit operation at 16nm HP technology file. In transient characteristics, it can be seen that dynamic power is dissipated during a transition from low to high or high to low. It shows alternative up and down peaks showing the alternate MOS device in operation. Spikes can be further reduced by increasing the rise time and fall time. Above results are obtained by setting rise time and fall time to 15ns.

4 CONCLUSIONS

In order to achieve ultra low power dissipation, circuits must be designed to operate under sub threshold region, but that may degrade performance of the device. It was observed that using DTMOS one may improve the characteristics and further reduce the power dissipation. In this paper we compare the power at different technology files. It is observed that as voltage is scaled

Table 1 Comparison table of Design for different library files

S. NO.	Length (nm)	W_p(nm)/ W_n(nm)	V_{dd} (V)	Power (nW)	Delay (ns)	Device Size = $(n+p)l^2$ nm^2
1	90	0.25/ 0.10	0.2	1.22	8.645	0.00283
			0.3	10.2	3.245	

			0.4	67.22	1.635	
2	65	0.196/ 0.07	0.2	0.771	10.165	0.00112
			0.3	6.45	4.505	
			0.4	42.6	1.99	
3	45	0.175/ 0.05	0.2	0.4168	14.425	0.00045
			0.3	3.48	5.66	
			0.4	23.31	2.58	
4	32	0.11725/ 0.035	0.2	0.2469	20.52	0.00015
			0.3	2.09	6.65	
			0.4	14.15	3.2	
5	22	0.012/ 0.027	0.2	0.3605	17.225	0.00002
			0.3	2.39	6.485	
			0.4	14.960	3.035	
6	16	0.037/ 0.018	0.2	0.2676	25.255	0.00001
			0.3	2.890	9.46	
			0.4	24.480	2.295	

down for the same technology delay is increased and as technology is also scaled down delay further increases due to more prominent parasitic components. It was also observed that if we maintain width of PMOS device less than NMOS device we can decrease this propagation delay at the cost of noise margin and symmetry. This can be observed in simulation results as we go down from 22nm to 16nm with different device sizing delay is not increased rather we managed to maintain delay through device sizing. For some application we may require that device have unequal noise margin, under that case we may vary the device sizing to obtain desired results.

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